REMARKS

The present application was filed on April 6, 2007 with claims 1-31. Claims 1-31 remain pending.

In the present Office Action, the Examiner has objected to claims 6 and 16 as being dependent upon a rejected base claim, but indicates they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Examiner has also rejected claims 1-5, 7-15 and 17-31 under 35 U.S.C. §103(a) as being unpatentable over Reiner (WO 2004/053889) in view of Lee (United States Patent No. 5,257,225) and Doyle et al. (U.S. Publication: "Characterization of Oxide Trap and Interface Trap Creation During Hot-Carrier Stressing of n-MOS Transistors Using the Floating-Gate Technique"; hereinafter Doyle).

In this response, Applicants respectfully traverses the rejections. Applicants respectfully request reconsideration of the present application in view of the remarks to follow.

Independent Claims 1, 11, 21, 24 and 27

Independent Claims 1, 11, 21, 24 and 27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Reiner in view of Lee and Doyle et al. Regarding claim 1, the Examiner asserts that Reiner discloses programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistors (FIG. 1 shows memory transistor T2; page 5, line 16, to page 6, line 19, discloses thermally damaging the drain junction of T2 by inducing hot carriers at the drain/oxide/gate junction). The Examiner acknowledges that Reiner does not expressly disclose wherein the injection of carriers causes at least one of, the creation of traps, and the filling of traps, but asserts that Reiner teaches oxide breakdown as obviously induced by degradation by (a) a hot carrier mechanism (trapping electrons; page 7, lines 7-11), that Lee teaches "filling up the traps in the dielectric region (col. 4, line 67, to col. 5, line 2), and that Doyle teaches trap creation during hot-carrier stressing of n-MOS transistors (Abstract).

Applicants note that Reiner teaches:

> In an equally preferred embodiment of the invention, a programming voltage level above the normal operation voltage level is used, in order to keep the cell size reasonably small. *High voltage levels may result in a degradation of the memory device due to an increased heating of the carrier. Hot carrier effects*

*occur e. g. in strong pinch-off conditions in a transistor, which in turn occur with a high drain voltage and a moderate to low gate voltage at the transistor. It has thus to be ensured that no intolerable degradation of the memory circuitry occurs due to the proposed high programming voltage. Hot carrier conditions resulting in a degradation, however, are **avoided effectively** with the proposed programming cycle comprising a ramping down of the voltage applied to the gate of the memory transistor.*
(Page 3, line 31, to page 4, line 9; emphasis added.)

Contrary to the Examiner's assertion, Reiner does *not* disclose or suggest *programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor.* In fact, Reiner actually teaches away from the present invention by teaching to *avoid hot carrier conditions.*

Furthermore, in the text cited by the Examiner, Lee teaches that "the fact that wordline pulse 65 ramps up is significant is that the small Fowler-Nerdheim current at the beginning which fills up the traps in the thin dielectric region before the higher Fowler-Nerdheim current will reduce the stress on the tunneling window dielectric and improve the dielectric lifetime." (Col. 4, line 67, to col. 5, line 4.) Lee, however, does not disclose or suggest *programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor.*

Finally, Doyle does not disclose or suggest *programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor.*

Thus, even as combined in the manner suggested by the Examiner, Reiner, Lee and Doyle, alone or in combination, *do not teach every element of the independent claims.* Furthermore, based on the KSR considerations discussed hereinafter, the combination/modification suggested by the Examiner is not appropriate.

<u>KSR</u> Considerations

An Examiner must establish "an apparent reason to combine … known elements." *KSR International Co. v. Teleflex Inc. (KSR)*, 550 U.S. ___, 82 USPQ2d 1385 (2007). Here, the Examiner merely states that it would have been obvious to incorporate the teachings (that the injection of carriers causes at least one of, the creation of traps, and the filling of traps) by Lee and Doyle in the cited claim limitation rejection. The Examiner asserts that the

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suggestion/motivation would have been obvious to one of ordinary skill in the art to conclude that (the) injection of carriers, as induced by voltage/current biasing of a transistor device, can cause oxide degradation resulting in charge trapping.

5 Applicants, however, are claiming a new technique for programming a one time programmable memory. There is no suggestion in Reiner, Lee and Doyle, alone or in combination, to *program* a transistor *using a hot carrier transistor aging technique to alter a characteristic of the transistor.*

Furthermore, Reiner's teaching to *avoid hot carrier conditions **teaches away*** from the present invention. The *KSR* Court discussed in some detail United States v. Adams, 383 U.S. 39 10 (1966), stating in part that in that case, "[t]he Court relied upon the corollary principle that when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious." (KSR Opinion at p. 12). Thus, there is no reason to make the asserted combination/modification.

In light of the above remarks and amendments, Applicants respectfully submit that claims 15 1-31 are in condition for allowance and request the withdrawal of the §103(a) rejections.

Respectfully submitted,

Kevin M. Mason

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Kevin M. Mason
20 Attorney for Applicant(s)
Reg. No. 36,597
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06824
25 (203) 255-6560